Abarajithan Gnaneswaran

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PhD candidate at UCSD, experienced in RTL/logic design, ASIC/FPGA implementation, firmware development, and training & optimizing ML models for embedded AI, via close collaboration with diverse teams of multiple disciplines, looking forward to contributing to the ongoing research and product development at your company.

EDUCATION

University of California, San Diego Sep 2022 - 2026 [anticipated]

- PhD candidate (Computer Engineering) at Kastner Research Group under Prof Ryan Kastner.
- Coursework (Fall): Princ. Comp. Arch, VLSI Digit Sys Algo & Arch, Low-power VLSI Implementation for ML

University of Moratuwa (Sri Lanka) Dec 2015 - Feb 2020

- BSc. (First Class Honors) in Electronics and Telecommunications Engineering
- GPA: 3.92/4.2 = 3.86/4.0, Deans List (3.8+) for 6/8 semesters
- **Thesis project:** Accelerating Object Detection (YOLOv2) on FPGA+ARM PSoC for Road Traffic Control, won gold in National & silver in Asia Pacific ICT Awards. Start-up and product development for govt.
- **Other projects:** System Bus with Priority Arbitration & Split Transactions; SOC to Apply Two 7x7 Kernels on 1080p 30 FPS YUV Stream; Custom CPU+ISA on FPGA Optimized for Image Processing.

SKILLS

Digital Design	SystemVerilog, TCL, Cadence Genus/Innovus/Virtuoso, Xilinx Vivado/Vitis
Machine Learning	PyTorch, Tensorflow, Keras, TensorRT (C++ & Python)
Programming	Python (Numpy stack, CocoTB), C/C++
Other	Git, CI/CD, LaTeX, ROS, AWS
Soft skills	Communication, presentation, teaching, teamwork & leadership

RELEVANT EXPERIENCE

RTL Design Engineer (R&D), Lemurian Labs (Canada) Dec 2020 - Aug 2022

- Designed & built the compute core to accelerate ML. Foundational work for the start-up, being taped-out now.
- Collaborated regularly with a multidisciplinary team of 12, spanning the globe: Designed & built arithmetic circuits for a novel Multidimensional Logarithmic Number System (MDLNS) with mathematicians, benchmarked them with physical designers, and worked closely with verification engineers to set up the testing framework.
- Evaluated trade-offs of 2D compression techniques & MDLNS on DNNs using PyTorch & NumPy with retraining.
- Set up CI/CD with automated smoke-test verification using CocoTB + iVerilog + Github Actions.

Lecturer on contract, University of Moratuwa (Sri Lanka) Aug 2020 - Apr 2021

- Designed new course EN3350: Software Design to industry demand; TA for DSP, Digital IC Design, SoC Design
- Publication: *A Mostly-Online CAS Teaching Experience*, C. Wijenayake, K. Wickremasinghe, G. Abarajithan, et al., IEEE International Symposium on Circuits and Systems (ISCAS), Austin Texas, USA, 2022

R&D Intern, CSIRO (Australia) Jul 2018 - Dec 2018

- Developed end-to-end pipeline for training DNNs using large datasets on a supercomputer, optimized (TensorRT) and deployed them on a robot running ROS on NVIDIA Jetson TX2, as initial work for DARPA SubT Challenge.

WEBINARS & TALKS

- **SystemVerilog for Digital Design, Synthesis & Simulation**, a self-initated series of 5 webinars I taught via simple → complex hands-on examples. 170+ participants, 2500+ downloads, overwhelmingly positive feedback.
- **Digital Design & Verification with SystemVerilog, Computer Architecture & ASIC Flow**, series of university short courses with Synopsys Collaboration (2023).
- **Modern C++: Clean & Performant Code**, talk in multiple workshops & university short courses
- **End-to-end pipeline for Embedded ML**, talk in university short course 'Embedded AI'

PROJECTS

Universal DNN Accelerator & Novel Dataflow enabling 70.7 Gops/mm2(int8) on TSMC 65nm

- 5.8× more Gops/mm2, 1.6× more Gops/W, higher MAC utilization, and fewer DRAM accesses than SOTA'21 (TCAS-1, TCOMP), processing AlexNet, VGG16 & ResNet50 at 336.6, 17.5 & 64.2 fps with 518.7 Gops.
- Unique dataflow eliminating need for local SRAMs inside processing elements, to fit 672 PEs (3.4×) in 7mm^2.
- PE array is primarily output-stationary, engine is also weight-stationary & input-stationary with respect to SoC.
- One-clock, on-the-fly reconfiguration of each pipeline stage using configuration header propagating along datapath.
- Elastic grouping: PEs dynamically regroup to maximize utilization for different kernel & channel sizes.
- Implemented with SystemVerilog, synthesized with Cadence Genus, place & route with Innovus.
- Quantized AlexNet, VGG16 & ResNet50 with PyTorch & Tensorflow to extract weights.
- LeakyRelu+Re-quantization Engine (RTL) to apply channel-wise & tensor-wise scales & biases between layers.
- Implemented a python testing framework to verify the hardware design against Tensorflow & Numpy results.
- Self-motivated passion project, open source

Object Detection with YOLOv2 & Road Traffic Control on Zynq Z7045 (FPGA+ARM PSoC)

- Won Asia-Pacific & national awards, founded start-up (web app) & product development (edge AI) for govt.
- Built 53 GFLOPS (float16) accelerator for 3x3 & 1x1 convolutional layers with 100% utilization.
- Built an AXI SoC around AXI-Stream accelerator, and developed C++ firmware to control AXI4 DMAs to run the 17 billion multiply-accumulates of the 21 conv2d layers in YOLOv2 & extract the vehicle bounding boxes.
- Built a keras-like custom inference framework using Numpy & experimented with custom-width floating points.
- Developed algorithms to track vehicles, calculate vehicle flow, speed & headway and get optimal signal timings.

A RISC processor in 99 lines of SystemVerilog

- Developed as a teaching tool for a university short course that I am leading with Synopsys collaboration, to introduce SystemVerilog, CompArch & ASIC flow to beginners & junior engineers.
- Complex enough to be interesting (eg: image processing), simple enough for beginners to comprehend.
- v1: single cycle, v2: 2-stage pipeline, v3: 6-stage pipeline, for same ISA & register set

System Bus & Protocol with Priority Arbitration & Split Transactions on FPGA

- Designed arbiter & custom protocols for masters, slaves & external devices & implemented on Altera DE2-115.
- External UART bus with custom auto baud rate detection protocol, tested on 3 FPGAs communicating in loop.

Custom CPU+ISA Optimized for Image Processing on FPGA

- Designed a custom ISA from mixed RISC & CISC principles for navigating around 2D arrays & processing them.
- Designed the CPU architecture & implemented on Altera DE2 115.
- Built an assembler and a cycle-accurate CPU simulator in python to accelerate algorithm development
- Developed algorithms for image upsampling, downsampling & edge detection and to apply custom RGB filters.

VOLUNTEERING

- **Co-Founder & Director of External Relations (2017-18) - Kavigai Foundation**, a non-profit to make quality secondary education accessible to students & teachers of underprivileged schools around Sri Lanka.

- **Sex Education & Awareness Workshops in Vietnam (2016)** as a team of local & international volunteers to educate school students on safe sex, LGBT rights and to prevent sexual harassment & human trafficking.

- **Electricity for Rual Houses & Energy Awareness Workshop for School Students (2017)**, collaborating with local & international volunteers. Raised funding, organized wiring program for rural houses in Sri Lanka.